

U.S.S.N. 10/761,657

Claim Amendments

Please amend claims 1, 11, 33, and 37 as follows:

Please cancel claim 19 as follows:

U.S.S.N. 10/761,657

Listing of Claims

1. (currently amended) A method for avoiding a step height over a readable laser marked portion of a process wafer comprising the steps of:

providing a process wafer comprising active area trenches and at least one inactive area trench formed overlying at least a portion of a laser marked portion at the process wafer periphery;

forming a filling layer over the active area trenches and the at least one inactive area trench to substantially fill the respective trenches;

~~forming a resist layer comprising patterned portions disposed between the active area trenches and the at least one inactive area trench;~~

forming a resist layer comprising first patterned portions and second patterned portions, said first patterned portions overlying the active area trenches and second patterned portions disposed between the active area trenches and the at least one inactive area trenches, said first and second patterned portions

U.S.S.N. 10/761,657

formed separately from one another;

removing the filling layer portions not covered by the resist layer;

removing the resist layer to expose remaining filling layer portions; and,

planarizing the wafer process surface including removing said remaining filling layer portions according to chemical mechanical polish (CMP) process wherein the active area trenches and the at least one inactive area trench including said laser marked portion are substantially co-planar.

2. (canceled)

3. (previously presented) The method of claim 1, wherein the step of removing the filling layer portions comprises a dry etching process.

4. (original) The method of claim 1, wherein the laser marked portion comprises an exclusion area at the process wafer periphery adjacent the process wafer peripheral edge.

U.S.S.N. 10/761,657

5. (original) The method of claim 1, wherein the active area trenches comprise shallow trench isolation (STI) trenches.

6. (original) The method of claim 1 wherein the process wafer comprises a silicon substrate and at least one overlying nitride layer.

7. (original) The method of claim 1, wherein the filling layer is selected from the group consisting of silicon dioxide and silicon oxynitride.

8. (original) The method of claim 1, wherein the patterned portions comprise a linear shape extending adjacent the length of the active area trenches.

9. (original) The method of claim 1, wherein the patterned portions comprise a width of greater than about 1.5 mm.

10. (original) The method of claim 9, wherein the patterned portions comprise at least two lines having a linewidth of from about 10 microns to about 500 microns with a pitch from about 1 to about 4 times the linewidth.

U.S.S.N. 10/761,657

11. (currently amended) A method for eliminating a step height over a readable laser marked portion of a process wafer to improve a subsequent patterning process over adjacent active areas comprising the steps of:

providing a process wafer comprising an active area including shallow trench isolation (STI) trenches and at least one trench formed in an adjacently disposed inactive area overlying a laser marked portion of the process wafer comprising readable information;

blanket depositing a layer of filling material over the process wafer surface;

forming a resist layer over comprising first patterned portions overlying the active area and an unpatterned portion overlying the inactive area;

lithographically patterning the resist layer to form second patterned portions disposed between the active area and the inactive area, said lithographically patterning comprising inserting a second mask comprising an image of the second

U.S.S.N. 10/761,657

patterned portions between the process wafer surface and a first mask comprising an image of the first patterned portions;

carrying out an etching process to etch through a thickness of exposed portions of the filling material according to the first and second patterned portions;

removing the resist layer; and

carrying out a CMP process to planarize the wafer process surface including the active area and the inactive area without an intervening step height.

12. (original) The method of claim 11, wherein the laser marked portion comprises an exclusion area at the process wafer periphery.

13. (original) The method of claim 11, wherein the process wafer comprises a silicon substrate and at least one overlying nitride layer.

14. (original) The method of claim 11, wherein the filling material is selected from the group consisting of silicon oxide

U.S.S.N. 10/761,657

and silicon oxynitride.

15. (original) The method of claim 11, wherein the first patterned portions comprise a reverse tone pattern.

16. (original) The method of claim 11, wherein the second patterned portions comprise lines extending adjacent the length of the active area.

17. (original) The method of claim 11, wherein the second patterned portions comprise a width of greater than about 1.5 mm.

18. (original) The method of claim 11, wherein the second patterned portions comprise at least two lines having a linewidth of from about 10 microns to about 500 microns with a pitch from about 1 to about 4 times the linewidth.

19. (cancelled)

20. (original) The method of claim 11, wherein the readable information is selected from the group consisting of alphanumeric characters, numbers, and bar codes.

U.S.S.N. 10/761,657

Claims 21-32 cancelled

33. (currently amended) A method for avoiding a step height over a readable laser marked portion of a process wafer comprising the steps of:

providing a process wafer comprising active area trenches and at least one inactive area trench formed overlying at least a portion of a laser marked portion;

forming a filling layer over the active area trenches and the at least one inactive area trench to substantially fill the respective trenches;

forming a resist layer comprising ~~linear~~ first patterned portions according to a first mask, said first patterned portions disposed between the active area trenches and the at least one inactive area trench;

then patterning the resist layer to form second patterned portions according to a second mask, said second patterned portions disposed between the active area and the inactive area;

U.S.S.N. 10/761,657

removing the filling layer portions not covered by the resist layer;

removing the resist layer; and,

planarizing the wafer process surface wherein the active area trenches and the at least one inactive area trench are substantially co-planar.

34. (previously presented) The method of claim 33, wherein the planarization process comprises a chemical mechanical polish (CMP) process.

35. (previously presented) The method of claim 33, wherein the step of removing the filling layer portions comprises a dry etching process.

36. (previously presented) The method of claim 33, wherein the linear first patterned portions comprise a linear shape extending adjacent the length of the active area trenches.

37. (currently amended) A method for avoiding a step height over a readable laser marked portion of a process wafer comprising the

U.S.S.N. 10/761,657

steps of:

providing a process wafer comprising active area trenches and at least one inactive area trench formed overlying at least a portion of a laser marked portion;

forming a filling layer over the active area trenches and the at least one inactive area trench to substantially fill the respective trenches;

forming a resist layer comprising first patterned portions overlying the active area, and an unpatterned portion overlying the inactive area, and a second patterned portion between the active area trenches and the at least one inactive area trench, said first and second patterned portions formed separately according to a first and a second mask;

removing the filling layer portions not covered by the resist layer;

removing the resist layer; and,

planarizing the wafer process surface wherein the active

U.S.S.N. 10/761,657

area trenches and the at least one inactive area trench are substantially co-planar.

38. (previously presented) The method of claim 37, wherein the planarization process comprises a chemical mechanical polish (CMP) process.

39. (previously presented) The method of claim 37, wherein the step of removing the filling layer portions comprises a dry etching process.

40. (previously presented) The method of claim 37, wherein the second patterned portion comprises a linear shape extending adjacent the length of the active area trenches.